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10/676,929	09/30/2003	Amit Singh	X-1495 US	7851

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EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/676,929	SINGH, AMIT
	Examiner	Art Unit
	Tuyen To	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/30/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *12-17 and 24-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-10,18-20 and 22* is/are rejected.

7)☒ Claim(s) *6,11,21 and 23* is/are objected to.

8)☒ Claim(s) *12-17 and 24-28* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/30/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/21/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 09/30/2003. Claims 1-28 are pending.

Election/Restrictions

1. During a telephone conversation with Dr. Kim Kanzaki (Reg. No. 37,652) on 09/23/2005, a provisional election was made **with traverse** to prosecute the invention of **group I (claims 1-11 and 18-23).** Affirmation of this election must be made by applicant in replying to this Office action. **Claims 12-17 and 24-28 are withdrawn** from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

2. This application contains claim groups directed to the following patentably distinct species of the claimed invention:

Groups:

Group I. **(Claims 1-11 and 18-23)** drawn to invention

with "packing, clustering, and placing components" steps,

without "first and second slices" for clustering, without "time-driven" placement.

Group II. **(Claims 12-17) drawn to invention (compared to Group I and III)**

with a different method used to implement the clustering process;

with "first and second slices", "a most critical attraction" ,

without "packaging" and "placing components",

without non-timing/timing driven placement.

Group III. **(Claims 24-28) drawn to invention (compared to group I and II)**

a different method used for placement

with "time-driven" placement,

without "identifying first and second slices" for the clustering process.

3. Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claims are generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election. Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a). Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement is traversed (37 CFR 1.143).

Applicant is advised that cancellation of non-elected claims is required.

Claim Objections

4. **Claim 1** is objected to because the claim recites "*to minimize critical connection* " without clearly defining what does it meant to minimize? Is it to minimize a number of critical connections or a timing delay of the critical connections?

5. **Claims 4 and 19** are objected to because in claims 4 and 19, the recited "combining slices that share control signals and clock sources " (to form what circuit?) needs clarification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 1-3, 7, 10, and 18** are rejected under 35 U.S.C. 102(e) as being anticipated by Wu et al. (US Patent No. 6813754).

Referring to claim 1, Wu et al. disclose a method of physical circuit design comprising the steps of:

packing components of a circuit design that are dependent upon an architecture of the circuit design (*Fig. 2; col. 3, lines 21-45; Fig. 3, col. 3 , lines 63+; col.4, lines 1-13*);

assigning initial locations to components of the circuit design (*Fig. 2; col. 3, lines 21-45; Fig. 3, col. 3 , lines 63+; col.4, lines 1-13);*

clustering a plurality of components of the circuit design according to design constraints (*Fig. 2; col. 3, lines 21-45; Fig. 3, col. 3 , lines 63+; col.4, lines 1-13*); and

placing the components of the circuit design to minimize critical connections (*Fig.4, col. 4, lines 14-56).*

Referring to claim 2, Wu et al. disclose the method of claim 1, wherein said clustering step operates on components that are not dependent upon the architecture of the circuit design (*col. 3, lines 40-45; Wu et al. discloses after a placement (step 206), each CLB may have: unassigned clusters (i.e. the clusters are not depended on a circuit architecture)).*

Referring to claim 3, Wu et al. disclose the method of claim 1, wherein said step of assigning initial locations is not timing driven (*in col. 7, lines 10-17, Wu el al. also disclose that the method ~~be ean~~ can be applied to alternative constraints such as power, routing congestion, or routing overlapped).*

Referring to claim 7, Wu et al. disclose the method of claim 1, said clustering step further comprising the step of adding a slice to a configurable logic block if the slice has a critical attraction to a slice already included in the configurable logic block (*col. 4, lines 29-56*).

Referring to claim 10, Wu et al. disclose the method of claim 9, further comprising the step of repeating said steps (a)-(e) for further critical connections (*Fig. 4, col.4, lines 29-62*).

Referring to claim 18, Wu et al. disclose a system (*col. 7, lines 25-45*) for physical circuit design comprising:

means for packing components of a circuit design that are dependent upon an architecture of the circuit design (*Fig. 2; col. 3, lines 21-45; Fig. 3, col. 3 , lines 63+; col.4, lines 1-13*);

means for assigning initial locations to each component of the circuit design (*Fig. 2; col. 3, lines 21-45; Fig. 3, col. 3 , lines 63+; col.4, lines 1-13*);

means for clustering the components of the circuit design by combining slices and including slices into configurable logic blocks according to design constraints (*Fig. 2; col. 3, lines 21-45; Fig. 3, col. 3 , lines 63+; col.4, lines 1-13*);

means for placing the components of the circuit design to minimize critical connections (*Fig.4, col. 4, lines 14-56*);

means for declustering the circuit design; and performing additional post-placement placer tasks on the declustered circuit design *(Fig. 3,col. 4, lines 1-4).*

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a), which forms the basis for all obviousness rejections, set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 4, 8, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (US Patent No. 6813754) in view of Chen et al. (US Patent No. 5475830).

Referring to claim 4 and similarly recited 19, Wu et al. disclose substantially all the elements in claim 1 except said clustering step further comprising the step of combining slices that share control signals and clock sources such that the total number of components of the combined slice does not exceed a threshold number of components.

Chen et al. disclose the method of clustering storages instances that share data paths ("control signals") and clock paths ("clock sources") (*col. 2, lines 30-38; Fig. 6, col. 13, lines 58+ to col. 14, lines 1-21; Fig. 11a, col. 14, lines 18-21*) such that each cluster should include a number of components no larger than the threshold size which can be handle by a programmable circuit device (*col. 14, lines 28-30*)

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the clustering step taught by Wu et al. with that of Chen et al. to thereby for the number of combined components (or slice) including in a cluster does not exceed the maximum number of components which the cluster can handle (*col. 14, lines 28-30*).

Referring to claim 8, **Wu et al**. disclose substantially the method of claim 1, except

said clustering step further comprising the step of using fanout to determine which slice is included in a configurable logic block if more than one slice to be added to the configurable logic block has an equivalent critical attraction to a slice within the configurable logic block.

Chen et al. disclose the step of using the criteria of the most fanout of a net that connects between components to determine which component in an oversized cluster to be selected into a smaller cluster (*col. 14, lines 28-44*).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the clustering step taught by Wu et al. with that of Chen et al. to thereby for the

number of combined components (or slice) including in a cluster does not exceed the maximum number of components which the cluster can handle (*col. 14, lines 28-30*).

Claims 5, 9, 20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wu et al.** (US Patent No. 6813754) in view of **Russo et al.** entitled A computer-based-design approach to partitioning and mapping of computer logic graphs (Proceedings of the IEEE Volume 60, Issue 1, Jan. 1972 Page(s): 28 – 34).

Referring to claim 5 and similarly recited 20, Wu et al. disclose substantially the method of claim 1, further comprising:

declustering the circuit design (*Fig. 3, col. 4, lines 1-4*); and

performing post-placement tasks on the declustered circuit design (*Fig. 3, col. 4, lines 1-4*); and

However, **Wu et al.** do not disclose wherein said clustering step further comprising including slices in a configurable logic block if the total number of inputs and outputs of the resulting configurable logic block does not exceed a threshold number of inputs and outputs.

Russo et al. disclose a partitioning (or "clustering") and mapping of logic blocks wherein one constraint required for a partition of logic blocks to be acceptable is that a total number of external connections (or I/O pins) should be equal or less than (or " not exceed") an external connection capacity (or " a threshold number of inputs and outputs") (*see Fig. 1; page 28*).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the clustering step taught by Wu et al. with that of Russo et al. to thereby for satisfying a design constraint on the pin capacity of configurable logic blocks (*page 28*).

Referring to claim 9 and similarly recited claim 22, Wu et al. disclose substantially the method of claim 1, said clustering step further comprising the steps of:

(a) selecting a critical connection of the circuit design (*Fig. 4; col. 4, lines 29-62*);

(b) identifying a first slice connected to the critical connection (*Fig. 4; col. 4, lines 29-62);*

(c) if the first slice is not clustered, identifying a second slice having a most critical attraction to the first slice (*Fig. 4, col.4, lines 29-62*);

(e) repeating steps (a), (b), (c), and (d) for further slices connected to the critical connection (*Fig. 4, col.4, lines 29-62*).

However, **Wu et al**. do not disclose the step (d) including the second slice with the first slice in a configurable logic block if the total number of inputs and outputs of the resulting configurable logic block does not exceed a threshold number of inputs and outputs; and

Russo et al. disclose a partitioning (or "clustering") and mapping of logic blocks wherein one constraint required for a partition of logic blocks to be acceptable is that a total number of external connections (or I/O pins) should be equal or less than (or " not exceed") an external connection capacity (or " a threshold number of inputs and outputs") (*see Fig. 1; page 28*).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the clustering step taught by Wu et al. with that of Russo et al. to thereby for satisfying a design constraint on the pin capacity of configurable logic blocks (*page 28*).

Allowable Subject Matter

10. **Claims 6, 11, 21, and 23** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. **Claims 6, 11, 21 and 23** would be allowable because the prior art of record does not teach or fairly suggest the limitations in:

wherein the threshold number of inputs and outputs is less than the number of inputs and outputs that can physically be accommodated by the configurable logic block so as to leave white space in the configurable logic block for post-placement circuit optimizations.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To

Patent Examiner

AU 2825

VUTHE SIEK
PRIMARY EXAMINER